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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/749,271
Filing Date: December 30, 2003
Appellant(s): HAMMARLUND ET AL.

Sumit Bhattacharya, Reg. No. 51,469
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 5/28/2008 appealing from the Office action mailed 9/6/2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

Merchant et al. (6,385,715), Merchant et al. (6,163, 838), herein "838", and Topham et al. (U.S. 6,944,853) are relied upon as evidence.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Maintained Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-2, 4, and 7 are rejected under 35 U.S.C. §102(b) as being anticipated by Merchant et al. (U.S. 6,385,715).

3. As per claim 1:

Merchant disclosed an adaptive replay system comprising:

A staging unit to forward an instruction in a replay loop parallel to an execution unit (Merchant: Figure 1 elements 117, 156, and 170, column 5 lines 16-40)(The staging unit is made up of staging queues A-F and the replay queue of the replay system 117. The replay loop is made of two converging loop paths. The first loop path is staging queues A-F and the second loop path is staging queues A-D and the replay queue.);

A selector device coupled to said staging area to place said instruction in an optimal position within said replay loop (Merchant: Figure 1 elements 150 and 154, column 6 lines 7-25)(Elements 150 and 154 are combined to read upon a selector device. The replay queue loading controller determines if the instruction is to be placed in the staging queues E and F or in the replay queue. The optimal position for the

instruction is based on its placement within either the staging queues or the replay queue of the replay loop.); and

A scoreboard coupled to said selector device to store status information for said instruction (Merchant: Figure 1 element 140, column 5 lines 50-59)(The scoreboard is coupled to the selector device, which is the checker and replay queue loading controller.).

4. As per claim 2:

Merchant disclosed the system of claim 1 wherein said staging unit is comprised of multiple stages (Merchant: Figure 1 element 139, column 5 lines 16-30)(The staging queues A-D.).

5. As per claim 4:

Merchant disclosed the system of claim 2 wherein said multiple stages are equivalent in number to a number of stages in said execution unit (Merchant: Figure 1 element 139, column 5 lines 16-30)(It's inherent that the stages are equal so that scheduled instructions can be matched with the checker for possible retirement.).

6. As per claim 7:

Merchant disclosed the system of claim 1 wherein said selector device is to analyze at least one instruction per clock cycle to determine whether said at least one instruction has executed correctly (Merchant: Figure 1 element 150, column 6 lines 7-25)(The checker determines if the instruction has executed correctly.).

Maintained Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 3, 9-15, 18-23, 25-27, and 29-30 are rejected under 35 U.S.C. §103(a) as being unpatentable over Merchant et al. (U.S. 6,385,715).

9. As per claim 3:

Merchant disclosed the system of claim 1 wherein said status information is latency (Merchant: Figure 1 element 154, and column 9 lines 1-24)(The replay queue loading controller checks to see if an instruction is going to be a short or long latency instruction. It would have been obvious to one of ordinary skill in the art at the time of the invention that this information could also be stored within the scoreboard. In addition, according to "In re Japikse" (181 F.2d 1019, 86 USPQ 70 (CCPA 1950)), shifting the location of parts doesn't give patentability over prior art.), dependency, and resource conflict information (Merchant: Figure 1 element 140, column 5 lines 50-59)(A resource conflict can be a register dependency because a resource the instruction needs is not available. This can be checked for within the scoreboard.).

10. As per claim 9:

Merchant disclosed the system of claim 1 wherein said selector device places said instruction in said optimal position within said replay loop based on status information for said instruction stored in said scoreboard (Merchant: Figure 1 element 154, column 9 lines 1-24)(The optimal position is selected based on latency information

from element 154. However, it would have been obvious to one of ordinary skill in the art at the time of the invention that the latency information could have instead been stored within the scoreboard. In addition, according to "In re Japikse" (181 F.2d 1019, 86 USPQ 70 (CCPA 1950)), shifting the location of parts doesn't give patentability over prior art.).

11. As per claim 10:

Merchant disclosed the system of claim 9 wherein said selector device can move instructions at least one position relative to a current position to said optimal position in said replay loop (Merchant: Figure 1 element 154, column 9 lines 1-24)(The replay queue loading controller has the effect of moving instructions up in their current position by putting them into the staging queues. When put in the staging queues, they can bypass those instructions that have longer latencies.).

12. As per claim 11:

Merchant disclosed the system of claim 3 wherein said scoreboard stores latency and dependency information for said instruction when said instruction is first scheduled, and updates latency and dependency information for said instruction when said instruction is executed (Merchant: Figure 1 element 140, column 5 lines 50-59)(The dependency information is updated to show if data sources were correct or not.) (Merchant: Figure 1 element 154, and column 9 lines 1-24)(The replay queue loading controller checks to see if an instruction is going to be a short or long latency instruction. It would have been obvious to one of ordinary skill in the art at the time of the invention that this information could also be stored within the scoreboard. It would have been

obvious to one of ordinary skill in the art that the latency information of load instructions would be updated upon cache misses. In addition, according to "In re Japikse" (181 F.2d 1019, 86 USPQ 70 (CCPA 1950)), shifting the location of parts doesn't give patentability over prior art.).

13. As per claim 12:

Merchant disclosed the system of claim 3 wherein said scoreboard stores resource conflicts for said instruction when said instruction encounters a resource conflict during execution (Merchant: Figure 1 element 140, column 5 lines 50-59)(A resource conflict can be a register dependency because a resource the instruction needs is not available. This can be checked for within the scoreboard. A resource conflict inherently occurs during execution with the checker determining if the correct data sources were used.)

14. As per claim 13:

Claim 13 essentially recites the same limitations of claim 1. Claim 13 additionally recites the following limitations:

A multiplexer having a first input, a second input, and an output (Merchant: Figure 1 element 116)(The MUX contains 3 inputs and one output. However, it would have been obvious to one of ordinary skill in the art that another MUX could be placed within the replay system to select between an instruction from the staging queues and from the replay queue. It would have been obvious to one of ordinary skill in the art that the replay MUX output would feed a 2-input, 1-output MUX that selects between the scheduler and the replay system. One of ordinary skill in the art would look to figure 6

and see that this is the implementation for multiple threads and could also be transferred to a system without multithreading capability. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention that the MUX could be modified to select between the scheduler and the replay system);

A scheduler coupled to said multiplexer first input (Merchant: Figure 1 element 114, column 3 lines 59-65);

An execution unit coupled to said multiplexer output (Merchant: Figure 1 element 118, column 4 lines 8-19);

A memory device coupled to said execution unit (Merchant: Figure 1 element 120, column 4 lines 8-19); and

A replay system having an output coupled to said second multiplexer input (Merchant: Figure 1 element 117, column 5 lines 16-30).

15. As per claim 14:

Claim 14 essentially recites the same limitations of claim 2. Therefore, claim 14 is rejected for the same reasons as claim 2.

16. As per claim 15:

Claim 15 essentially recites the same limitations of claim 3. Therefore, claim 15 is rejected for the same reasons as claim 3.

17. As per claim 18:

Claim 18 essentially recites the same limitations of claim 7. Therefore, claim 18 is rejected for the same reasons as claim 7.

18. As per claim 19:

Claim 19 essentially recites the same limitations of claim 9. Therefore, claim 19 is rejected for the same reasons as claim 9.

19. As per claim 20:

Claim 20 essentially recites the same limitations of claim 10. Therefore, claim 20 is rejected for the same reasons as claim 10.

20. As per claim 21:

Claim 21 essentially recites the same limitations of claim 11. Therefore, claim 21 is rejected for the same reasons as claim 11.

21. As per claim 22:

Claim 22 essentially recites the same limitations of claim 12. Therefore, claim 22 is rejected for the same reasons as claim 12.

22. As per claim 23:

Merchant disclosed a method of processing a computer instruction in a replay loop comprising:

Analyzing multiple instructions from a staging unit (Merchant: Figure 1 element 139, column 5 lines 16-30)(There are multiple instructions within the staging unit that will be analyzed to see if they correctly executed or not.);

Checking a scoreboard for latency information for each of said multiple instructions (Merchant: Figure 1 element 154, column 9 lines 1-24)(The replay queue loading controller checks to see if an instruction is going to be a short or long latency instruction. It would have been obvious to one of ordinary skill in the art at the time of the invention that this information could also be stored within the scoreboard. In

addition, according to "In re Japikse" (181 F.2d 1019, 86 USPQ 70 (CCPA 1950)), shifting the location of parts doesn't give patentability over prior art.);

Checking for dependency information for each of said multiple instructions (Merchant: Figure 1 element 140, column 5 lines 50-59);

Checking said scoreboard for resource conflicts for each of said multiple instructions (Merchant: Figure 1 element 140, column 5 lines 50-59)(A resource conflict can be a register dependency because a resource the instruction needs is not available. This can be checked for within the scoreboard.);

Determining an optimal position for each of said multiple instructions in said replay loop (Merchant: Figure 1 element 154, column 6 lines 7-25)(The replay queue loading controller determines if the instruction is to be placed in the staging queues or in the replay queue. The optimal position for the instruction is based on its placement within either the staging queues or the replay queue.); and

Moving each of said instructions to said optimal position in said replay loop (Merchant: Figure 1 element 154, column 6 lines 7-25)(The replay queue loading controller determines if the instruction is to be placed in the staging queues or in the replay queue. The optimal position for the instruction is based on its placement within either the staging queues or the replay queue.).

23. As per claim 25:

Claim 25 essentially recites the same limitations of claims 3 and 9. Therefore, claim 25 is rejected for the same reasons as claims 3 and 9.

24. As per claim 26:

Claim 26 essentially recites the same limitations of claim 10. Therefore, claim 26 is rejected for the same reasons as claim 10.

25. As per claim 27:

Claim 27 essentially recites the same limitations of claim 23. Therefore, claim 27 is rejected for the same reasons as claim 23.

26. As per claim 29:

Claim 29 essentially recites the same limitations of claims 3 and 9. Therefore, claim 29 is rejected for the same reasons as claims 3 and 9.

27. As per claim 30:

Claim 30 essentially recites the same limitations of claim 10. Therefore, claim 30 is rejected for the same reasons as claim 10.

28. Claims 5-6 and 16-17 are rejected under 35 U.S.C. §103(a) as being unpatentable over Merchant et al. (U.S. 6,385,715), in view of Merchant et al. (U.S. 6,163,838), herein referred to as 838.

29. As per claim 5:

Merchant disclosed the system of claim 2.

Merchant failed to teach wherein said adaptive replay system is implemented within a multiple channel processor.

However, 838 disclosed wherein said adaptive replay system is implemented within a multiple channel processor (Merchant: Figure 3 element 50, column 5 lines 59-65).

Merchant is a continuation of 838. The advantage of using multiple channels is that performance will be increased by being able to execute additional instructions per cycle. Thus, it would have been obvious to one of ordinary skill in the art to look at 838 for additional details and find that the processor can include multiple channels.

30. As per claim 6:

Merchant disclosed the system of claim 5.

Merchant failed to teach wherein said selector device is to place said instruction in said optimal position within said replay loop, from a first channel to a second channel, based on status information for said instruction stored in said scoreboard.

However, it would have been obvious to one of ordinary skill in the art that multiple channels, or execution units could have the same functionality, such as an integer unit. It also would have been obvious to one of ordinary skill in the art that a replayed instruction could be scheduled to be executed on either integer unit. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention that the replayed instruction could change from a first channel to a second channel based on status information, which would tell that the instruction is to be replayed.

31. As per claim 16:

Claim 16 essentially recites the same limitations of claim 5. Therefore, claim 16 is rejected for the same reasons as claim 5.

32. As per claim 17:

Claim 17 essentially recites the same limitations of claim 6. Therefore, claim 17 is rejected for the same reasons as claim 6.

33. Claims 8, 24, and 28 are rejected under 35 U.S.C. §103(a) as being unpatentable over Merchant et al. (U.S. 6,385,715), in view of Topham et al. (U.S. 6,944,853).

34. As per claim 8:

Merchant disclosed the system of claim 7.

Merchant failed to teach wherein said selector device analyzes 3 instructions per clock cycle.

However, Topham disclosed wherein said selector device analyzes 3 instructions per clock cycle (Topham: Figure 1 elements 14-18, column 3 lines 25-42)(The combination of Topham and Merchant results in three execution units that are processing instructions per clock cycle. It would have been obvious to one of ordinary skill in the art at the time of the invention that the replay unit must add stages to keep track of the instructions from the new execution units and therefore analyzes 3 instructions per clock cycle to see if any of them can retire.).

The advantage of adding additional execution units is that it will increase the performance of the processor by executing additional instructions per cycle. The advantage of increased performance would have motivated one of ordinary skill in the art to implement additional execution units on the processor of Merchant. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to add additional execution units for the advantage of increased performance.

35. As per claim 24:

Claim 24 essentially recites the same limitations of claim 8. Therefore, claim 24 is rejected for the same reasons as claim 8.

36. As per claim 28:

Claim 28 essentially recites the same limitations of claim 8. Therefore, claim 28 is rejected for the same reasons as claim 8.

(10) Response to Argument

37. Regarding claims 1-2, 4, and 7 are rejected under 35 U.S.C. §102(b) as being anticipated by Merchant et al. (U.S. 6,385,715):

38. Applicant argues "Applicants submit the cited section does not teach the relevant limitations; indeed, the cited section does not refer to optimally rearranging the order of instructions at all."

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., rearranging the order of instructions) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

39. Applicant argues "Applicants submit at the heart of the cited section is this two-outcome *conditional determination* of where to send an instruction that hasn't executed properly. However, making a conditional determination upon which one of two steps

may be followed is not the same as placing an instruction in an optimal position *within a replay queue* (as described in embodiments of the present application) at all."

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., optimal position within a replay queue) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Instead, what is claimed is "an optimal position within said replay loop."

40. Applicant argues "Merchant failed to teach or suggest a selector device coupled to said staging area to place said instruction in an optimal position within said replay loop."

This argument is not found to be persuasive for the following reasons. Elements 150 and 154 from Merchant (U.S. 6,385,715) were cited for this limitation. Element 150 determines if a replay is necessary and element 154 determines which replay path of the replay loop will be used for the instruction. Element 154 places the instruction in an optimal position of the replay loop for the processor because it has the ability to put the instruction on the fast track for being replayed by sending it through staging queues E and F, as opposed to sending the instruction into the replay queue where it could be delayed much longer than two cycles.

The fast track within the replay loop, staging queues E and F, are the optimal position for short latency instructions to be re-executed within the processor (Merchant:

Column 6 lines 43-49). For long latency instructions, such as cache misses (Merchant: Column 7 lines 23-25), the optimal placement in the replay loop is within the replay queue path to avoid hundreds of wasted replay iterations of the instruction that resulted in a cache miss. Such a large number of executed iterations within the processor is a considerable waste of resources and power, which will also result in increased latency for the executed application (Merchant: Column 7 lines 43-63). Thus, for these long latency instructions, the optimal placement in the replay loop is to be placed in the replay queue path to avoid said waste of resources and power.

Therefore, Merchant correctly reads upon the claimed limitation by sending short latency instructions to their optimal placement in the replay loop via staging queues E and F and by sending long latency instructions to their optimal placement in the replay loop via the replay queue path.

The above argument also applies to other independent claims 13, 23, and 27.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/JAP/

/Jacob Petranek/

July 21, 2008

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